## REMARKS

### Amendment to the claims

Claim 1 has been clarified to recite that *"said first well is generally deeper than said first and second active regions"*. Applicants note that this clarification is supported by the specification as filed, for example the first paragraph of page 11, which recites that *"a well implant is generally deeper than the source/drain implants"*, and is not a limitation on the scope of the claim.

Applicants respectfully submit that no new search is required in view of the above amendment, which only relates to reciting implicit features in explicit language.

Applicants note that it is basic knowledge in the field of semiconductors that "well" is commonly defined as an "implanted/diffused region in Si wafer needed to implement complementary MOS (CMOS) cell; depending on the design either n-well or p-well is used".

(see http://semiconductorglossary.com/default.asp?searchterm=well)

It is also basic knowledge in the field of semiconductors that a well (n-well or p-well) in a CMOS cell has known structural features that allow the well to have known technical effects on the active regions of the CMOS cell.

For example, the firm Cadence Design Tools, in a basic Internet tutorial related to CMOS layout, describes an n-well as a "larger n-type region" that "acts like a substrate for the PMOS transistors".

(see http://www.vlsi.wpi.edu/cds/examples/layout.11.html)

It follows in particular that any "well" as commonly known in the field of semiconductors has a depth and concentration enabling the region to act "like a substrate" for active regions formed in it (i.e. generally deeper than the source/drain implants). Thus reciting that the *"first well is generally deeper than said first and second active regions"* is merely an explicit recitation of implicit features.

The Applicants bring to the attention of the Examiner that the above clarification was introduced in claim 1 of the corresponding U.K. patent application No. 0,512,203.1 to help distinguishing unambiguously U.K. claim 1, which had a language identical to pending claim 1, from prior art references cited by the U.K. Examiner.

In particular, Applicants submit that claim 1 is patentable over U.S. 5,146,117 to Hughes by Larson (D1); EP 0528302 to Hughes by Walden (D2); JP 2188944 to Sharp by Kono (D3); U.S. 6,326,675 to Philips by Scott (D4); and U.S. 4,766,516 to Hughes by Ozdemir (D5). Applicants note that Larson, Walden, Scott and Ozdemir were brought to the attention of the Examiner in the IDS dated May 21, 2004, and that Kono was brought to the attention of the Examiner in the IDS dated August 30, 2004.

Larson relates to a convertible camouflage circuit that can be argued to have an electrical path between active regions regardless of any reasonable voltage applied to the circuit. Larson discloses a circuit wherein ions are implanted in the channels regions of FET structures, for example so that the FET is constantly turned ON for all logical levels of applied gate voltage (col. 3, lines 45-51). Applicants note that Larson relates to a camouflaged circuit structure having a *ion implanted region* 54 disposed in a substrate under a gate region, wherein the *ion implanted region* 54 is too shallow to read on a well *"generally deeper"* than the active regions as recited in claim 1, whereby claim 1 is novel over Larson.

Walden relates to a camouflage structure where an altered gate switches in an

apparently normal manner when tested under DC or low speed conditions, but does not switch at normal operating speed (second sentence of the abstract). Applicants note that D2 fails to disclose an implanted channel (modified channel) 46c or 48c that would be generally deeper than the sources/drains 46a, 46b or 48a, 48b. Accordingly, Applicants respectfully submit that Walden fails to disclose a well *"generally deeper"* than the active regions, as recited in claim 1, whereby claim 1 is novel over Walden.

Kono relates to a camouflage structure involving for example a dummy P-type MOSFET 6 which is always in a conductive state irrespective of a level of a signal to be input from a dummy input terminal 16, a dummy P-type MOSFET comprising a P+ region 74 in the channel between P+ source and drain 71 and 72. Applicants respectfully submit that Kono fails to disclose or suggest a P+ region 74 that would read on a well *"generally deeper"* than the active regions, as recited in claim 1. Applicants therefore respectfully submit that at least in view of the above, claim 1 is novel over Kono.

Scott relates to a camouflage structure wherein a conducting lightly doped (NLDD) link is formed under an oxide spacer 18 between two active areas 10a and 12a (col. 4, lines 35-37). Applicants respectfully submit that Scott fails to disclose or suggest a conducting light doped link (LINK) that would be *"generally deeper"* than the active areas, whereby Scott fails to disclose or suggest a well *"generally deeper"* than the active regions, as recited in claim 1. Applicants respectfully submit that at least in view of the above, claim 1 is novel over Scott.

Ozdemir relates to a camouflage device wherein the channel (40) of a FET is doped to make the FET always conductive, to alter the device from a FET to a short circuit (col. 8, lines 62-65). Applicants respectfully submit that Ozdemir fails to disclose or suggest a channel 40 that would be *"generally deeper"* than the source/drain implants, whereby Ozdemir fails to disclose or suggest a well *"generally deeper"* than the active

regions, as recited in claim 1. Applicants therefore respectfully submit that at least in view of the above, claim 1 is novel over Ozdemir.

The Applicants note that none of the above references disclose a well *"generally deeper than said first and second active regions"* as recited in claim 1, whereby no combination of the cited references would have led a person skilled in the art to a circuit structure as recited in claim 1. Applicants therefore respectfully submit that claim 1 is inventive over any combination of Larson, Walden, Kono, Scott and Ozdemir.

No new matter has been added. Applicants expressly reserve the right to prosecute any matter cancelled from the claims in this application or in any derivative thereof.

Rejections under 35 U.S.C. 102

Claims 1 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,210,437 to Sawada. Applicants respectfully disagree.

Claim 1

In the present action, the Examiner seems to argue that there is no teaching in Sawada that the recited structure does not act as recited in the claim, and that furthermore, since the entire structure of Sawada is essentially identical to the structure shown in the application, it would be concluded that both structures would have the same electrical functions/effects. Applicants respectfully disagree with the Examiner.

The Applicants note for example that all the claims of Sawada relate to a circuit comprising a MOS transistor. It is known of the skilled reader, a specialist of

microelectronics, that a "transistor" does not provide an electrical path "regardless of any reasonable voltage applied to it", and it can in particular not be deemed to disclose or suggest a structure having a well that "*provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*" as recited in claim 1. The structure of claim 1 may look like a MOS transistor, but does not operate as a MOS transistor. As a matter of fact, the claimed structure precisely aims at looking like a transistor while not operating like one.

Accordingly, contrary to the Examiner's opinion, there is clear teaching in Sawada that the structure of Sawada does not operate like the recited structure. Indeed, by claiming a transistor, Sawada indicates that it is essential that its structure operates as a transistor, whereby Sawada teaches away from the claimed structure, which does not operate as a transistor. Despite any similarities that may exist between Sawada and the claimed features, Sawada actually teaches away from a camouflaged circuit structure as recited in claim 1.

At least in view of the above, Applicants respectfully submit that claim 1 is patentable over Sawada.

Should the Examiner be of the opinion that a "transistor" reads on a structure that provides an electrical path regardless of any reasonable voltage applied to it, the Applicants respectfully request the Examiner to provide an affidavit or declaration setting forth specific factual statements and explanation to support that a "transistor" reads on a structure that provides an electrical path regardless of any reasonable voltage applied to it, in compliance with 37 CFR 1.104(d)(2).

Claim 5

Claim 5 depends on claim 1. Applicants respectfully submit that at least in view of its dependency on claim 1, claim 5 is patentable over Sawada.

Rejections under 35 U.S.C. 103

Claims 2, 3 and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada in view of U.S. Pat. No. 3,938,620 to Spadea, and claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 4,860,084 to Shibata in view of U.S. Pat. No. 4,145,701 to Kawagoe. Applicants respectfully disagree.

Claims 2, 3 and 4

Claims 2, 3 and 4 depend directly or indirectly on claim 1. Applicants note that the Examiner has failed to show that Spadea shows a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*. In view of the above, Applicants submit that the Examiner has failed to show that Sawada or Spadea, alone or in combination, would have led one of ordinary skill to a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*. Accordingly, Applicants respectfully submit that claim 1 is patentable over Sawada in view of Spadea, and respectfully submit that at least in view of their dependency on claim 1, claims 2, 3 and 4 are patentable over Sawada in view of Spadea.

Claim 6

The Examiner opines that the combination of Kawagoe "may remove the contact portions of Shibata, however such a removal would still permit the combination of Shibata and Kawagoe to disclose the limitations in the applicant's claims since the

claims do not recite anything about contact portions". Applicants respectfully disagree with the Examiner.

Applicants note that they have not argued that the combination of Shibata and Kawagoe would fail to disclose contact portions.

Applicants have noted that one skilled in the art would have lacked motivation to combine Shibata and Kawagoe. Applicants respectfully remind the Examiner that M.P.E.P. 2143.01 (V) emphasizes that "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification". In the present case, Shibata relates to an improvement of the contact portions to connect elements with conductive wires, whereas Kawagoe, relates to suppressing such contact portions. Accordingly, the modification proposed by the Examiner would either render the prior art invention of Shibata or the prior art invention of Kawagoe unsatisfactory for its intended purpose. In particular, the modification suggested by the Examiner of removing the contact portions of Shibata would render Shibata unsatisfactory for its intended purpose of having fine contact portions to connect elements with conductive wires.

Applicants respectfully submit that at least in view of the above, claim 6 is patentable over Shibata and Kawagoe.

The Examiner further opines that "the inclusion of layers 78, 76 is still beneficial to Shibata since they would prevent leakage current to flow between a source and drain region in a substrate". Applicants respectfully disagree.

Applicants note that Shibata teaches (column 6, lines 38-51) that *"Since the V-shaped contact concave portions 22 and 72 surrounded by the p-type semiconductor layers (referred to as "p well regions" in this specification) 76 and 78 are formed on both sides of the*

*source and drain regions 12 and 14 of one MOS FET Q.sub.1, it is possible to prevent the occurrence of "punch through" which result in a leakage current flowing between the V-shaped contact concave portions 22 and 72. This is because a current loss from the n-type diffusion layers 24 and 74 to the substrate 10 can be reliably prevented since the concentration of p-type impurities is set to be high in the substrate portion which is in contact with the neighboring V-shaped n-type diffusion layers 24 and 74".*

The Examiner seems to rely on knowledge on his own to assert that without the V-shaped contact concave portion, there would be a leakage current between the source and drain, and that layers 78, 76 would prevent such leakage current to flow. Applicants note that Shibata expressly teaches that a leakage current would flow between the V-shaped contact concave portions 22 and 72 if it were not for the layers 78, 76. Applicants note that the Examiner has failed to explain what is the technical basis of the Examiner for asserting that, should the contacts (and consequently the V-shaped contact concave portions 22 and 72) be removed, there would be leakage current between the source and drain of Shibata. The Examiner has further failed to show:

-between which parts of the source and drain there would be a leakage current;

how the layers 78 and 76 would have to be disposed to prevent the occurrence of such leakage current; and

what basis supports such findings.

Since the examiner seems to be relying on personal knowledge to support that without the V-shaped contact concave portion, there would be a leakage current between the source and drain, and that layers 78, 76 would prevent such leakage current to flow, the Applicants respectfully request the Examiner to provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding, in compliance with 37 CFR 1.104(d)(2).

For the above reason also, Applicants submit that claim 6 is patentable over Shibata and Kawagoe.

* * *

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

February 19, 2007
(Date of Transmission)

Alma Smalling
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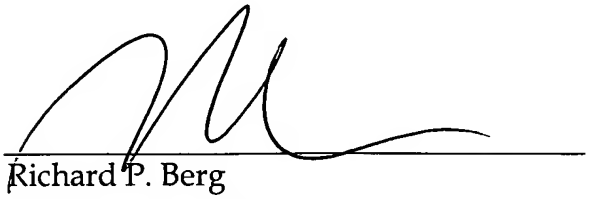
(Signature)

2/19/07
(Date)

Respectfully submitted,



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